Final report on policy recommendations

PACK4EU

Boost
Semiconductor
Packaging in Europe

Chips JU

Funded by
the European Union

The project is supported by the CHIPS-JU and its members

Abstract

The European semiconductor ecosystem must prioritize Packaging R&D to meet the diverse needs of sectors like automotive, telecom, industry, defense, aerospace, and medical. Innovation in semiconductor is shifting from front-end towards back-end processing with advanced packaging as a key game changer. To address the complexity and performance demands of modern devices, technologies such as 2.5D and 3D integration, chiplet architectures, and photonics are crucial. Applications like ADAS, AI or 6G telecommunications will need highly integrated systems with superior performance and efficiency, that will not be possible without advanced packaging technologies.

A first roadmap has been drafted, but industry and research engagement are needed. Challenges include a faster technology transfer from research to industry and the lack of open facilities for advanced packaging. Europe must invest in technology transfer and facilities, and enhance training programs to provide the necessary skilled workforce. Digitalization and sustainability present challenges and opportunities for collaboration e.g. on sustainable materials. SMEs need dedicated funding instruments to support their role in these strategic businesses, be it as technology providers or users. The Pack4EU initiative has for the first time successfully united the fragmented Packaging community across Europe and this network will continue beyond the end of the project.

9 recommendations are presented.

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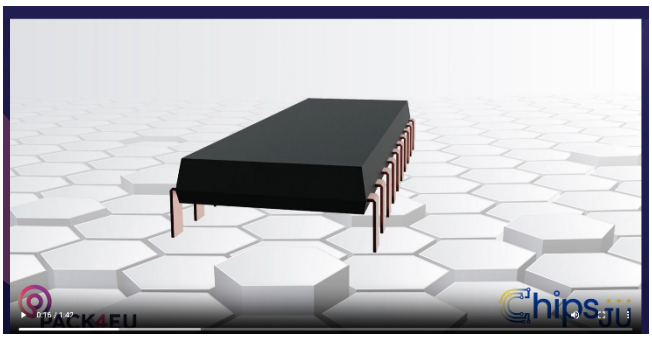
Foreword

This document is the publishable version of the final deliverable of the Pack4EU. The Pack4EU project was supported by the CHIPS Joint Undertaking and its members and worked from July 2023 to June 2024.

For readers who are not familiar with the technologies of Semiconductor Packaging and Advanced Packaging we recommend the short explanatory video available from the Pack4EU website: https://pack4eu.eu/ .



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Strategic Goal targeted by Pack4EU

The Mission of Pack4EU is to federate the European Packaging Industry to secure, revitalise and strengthen the advanced packaging capabilities in Europe.

The proposed vision is to unite the European Packaging industry on a common roadmap focused on Advanced Packaging. Semiconductor packaging is a commodity and is now produced in Asia with a high concentration of packaging services in Taiwan and China, cumulating 84% of the market shares (ref. Figure 1). The whole world is dependent on Asia for packaging and material supply, but Europe has maintained a strong R&D in this area.

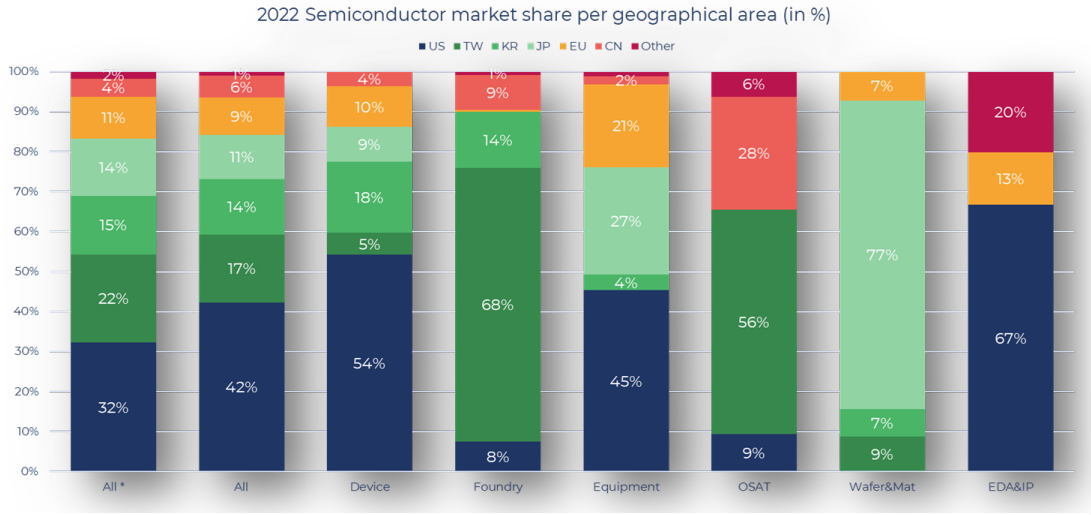

Figure 1: Breakdown of the Semiconductor market per geographical area - Source Yole développement. OSAT are concentrated in TW and CN, Material are concentrated in JP and SK

The Strategy proposed in this document is then aiming at the:

> Establishment of Advanced Packaging Capabilities in Europe for the European Market.

The strategy presented in this document is derived from a set of data collected from questionnaires (109 replies and growing), more than 50 interviews and nearly 20 workshops.

Strategic markets for Europe

In 2022, the revenue generated by Advanced Packaging was 47% of the total packaging market. By 2028, Advanced Packaging's revenue will increase to approximately 58% of the total packaging market (see Figure 2) while representing only 5% of the volume. The set of technology described under the label of "Advanced Packaging" receives a lot of traction from AI and computing and will reach other markets in the coming years.

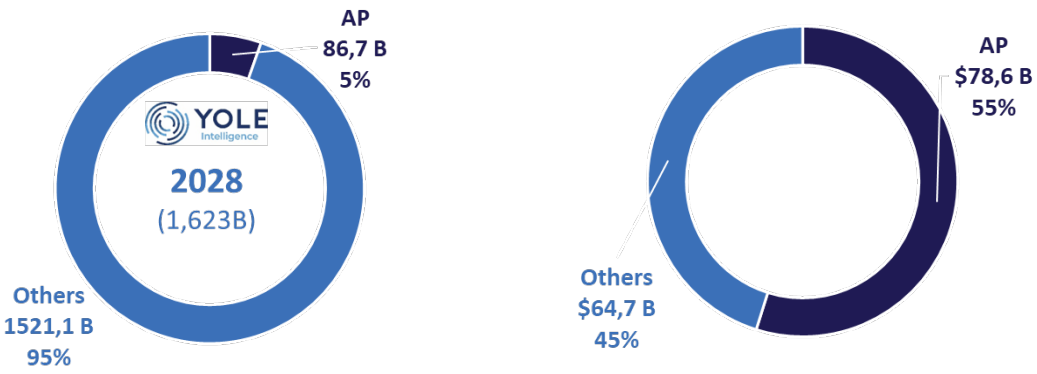

Figure 2: Advanced Packaging in volume (left) will reach 5% of market share for a value of 55% in 2028 (right) - Source Yole

The priority of our strategy is to serve the critical applications for Europe. Europe has a high-end positioning in Electronics and the key application markets are in Automotive, Telecom, Industry, Medical and also the so-called sovereign markets which include Defense and Aerospace applications.

- **Automotive** : the European packaging Market for automotive represents a value of **4,56B€**[1] and is critical for the European Economy. For the most optimistic scenario, **Automotive should adopt Advanced Packaging within 3 years.**

- **Telecom** – and more specifically the base station market where Europe **owns 42% of the market share generating a revenue of 21,5B€.** With European Champions like Ericsson and Nokia ranked respectively in 2nd and 3rd position and respective market shares of 25 and 17%. [1]

- **Industry** – Industry needs to reduce its impact on the environment and have a better control on its energy consumption. The digitalisation effort requires many sensors connected to edge computing capabilities leading to a highly fragmented need and market. Europe has a strong position in Sensors and the growth for Industrial MEMS sensors is reaching a double-digit figure with a CAGR of 13,27%.[1]

- **Sovereign markets:** Since 2014, Defense and Aerospace has been increasing in Europe with a total expenditure of 214B€ in 2021[1]. The strength in Europe are with Infrared players (Lynred,

[1] Yole Study for Pack4EU - p.101

Thales, Theon, Safran…), Tactical RF (Bittium, Saab Grintek, Thales). The total market is 690M$ with most of the components produced in Europe.

- **Medical** – Europe stands a strong presence with actors like Medtronic (13% market share), or Philips (9% market share) in a 530B$ global market. Siemens Healtineers holds a 14% market share in Medical Imaging Equipment market (40B$), and Biomérieux owns 13% of IVD and biology tools market (11B$). The needs of this market in terms of semiconductor is highly fragmented and can include MEMS component, High definition camera and Power electronics. It represents a market of 242M€ for packaging with a high mix.[1]

The worldwide need in packaging in these critical areas is presented in the Figure 3 as a percentage compared the rest of the world. In Figure 3 , the % of units should be understood as : the need of Europe in the field of Automotive represents 18% of the worldwide needs. To date, only the needs in defense are managed in Europe, all the other areas are in a large majority packaged in Asia.

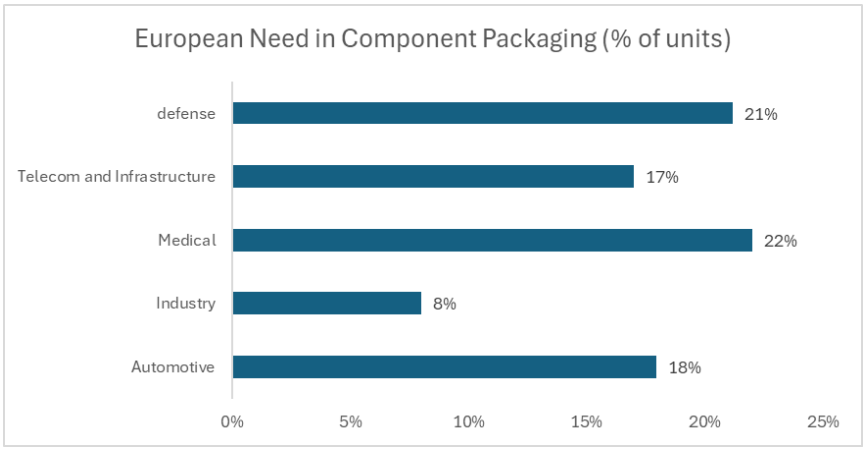

Figure 3: European need in packaging for the critical industries (% in number of units)

SWOT Analysis

In the Figure 4 we represent the status of Semiconductor Packaging in Europe both in the research area and industrial area.

Figure 4: Status of Semiconductor Packaging in Europe - SWOT analysis

The CHIPS JU tools

The European Chips Act of the European Union centers around three main pillars aimed at bolstering the semiconductor industry within Europe (Figure 5-Left). Firstly, it focuses on increasing investment in research and development to foster innovation and competitiveness in chip manufacturing. The second pillar aims to strengthen regulatory frameworks to support the growth of semiconductor production capacity within the EU, attracting "First of a kind investment". The 3rd pillar aims to enhance the resilience of supply chains by promoting strategic partnerships and reducing dependency on non-European sources for critical technologies.

Thanks to the pillar one, a large R&D investment program establishing Pilot Lines and a Design Platform is in progress and a recent press release confirmed that the ***"Chips Joint Undertaking (Chips JU) announces the successful evaluation of the submitted innovative semiconductor pilot line proposals and has started negotiations with four consortia, aiming at signing the relevant agreements later this year".*** A budget of 370M€ is dedicated to an advanced packaging Pilot Line and additional Pilot Lines are under discussion.

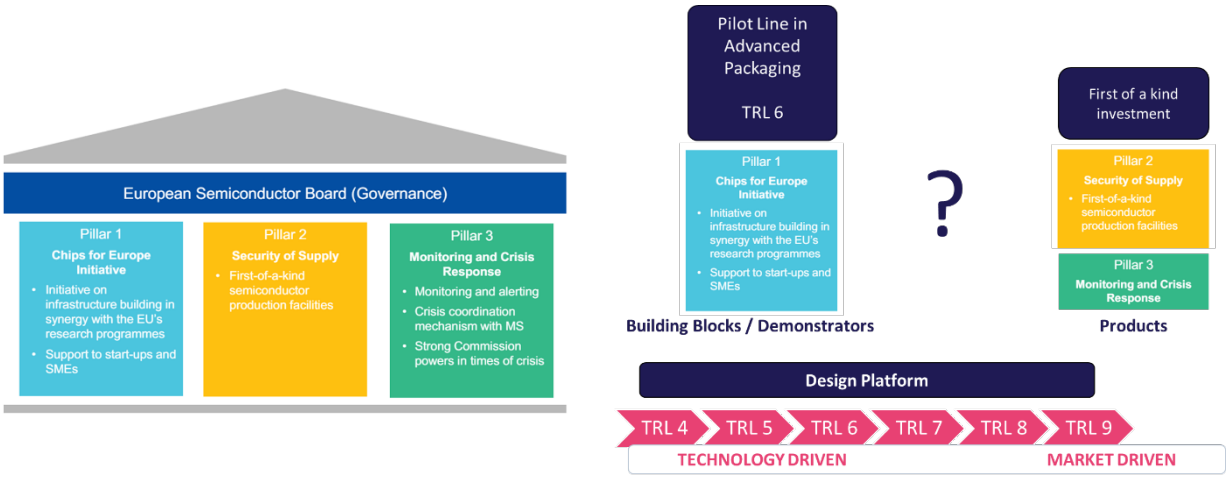

Figure 5: The 3 pillars of the Chips Act (left) re-organised according to the Technology Readiness Scale (right)

It is important to note that the Pillar 1 is focused on research and Pillar 2 and 3 are more focused on the supply chain. The actions conducted in the Pillar 1 are technology driven and aims to develop technology building blocks to be applied in a broad range of products. The actions in Pillar 2 have already led to the announcement of investments in both front-end and back-end facilities. These investments are market driven and appear disconnected from the Pillar 1.

It is expected that in the second half of 2024, a call for a Design Platform will open with the support of a Platform Coordination Team (PCT)[2]. The access to the Design Platform will be granted to SMEs either directly or through the support of Design Enablement Teams who will be certified by the PCT. The

[2] https://www.chips-ju.europa.eu/Chips-2024-CDP-1/

Design Platforms are key for packaging since the co-design of components in a chiplet architecture is a critical step in Advanced Packaging.

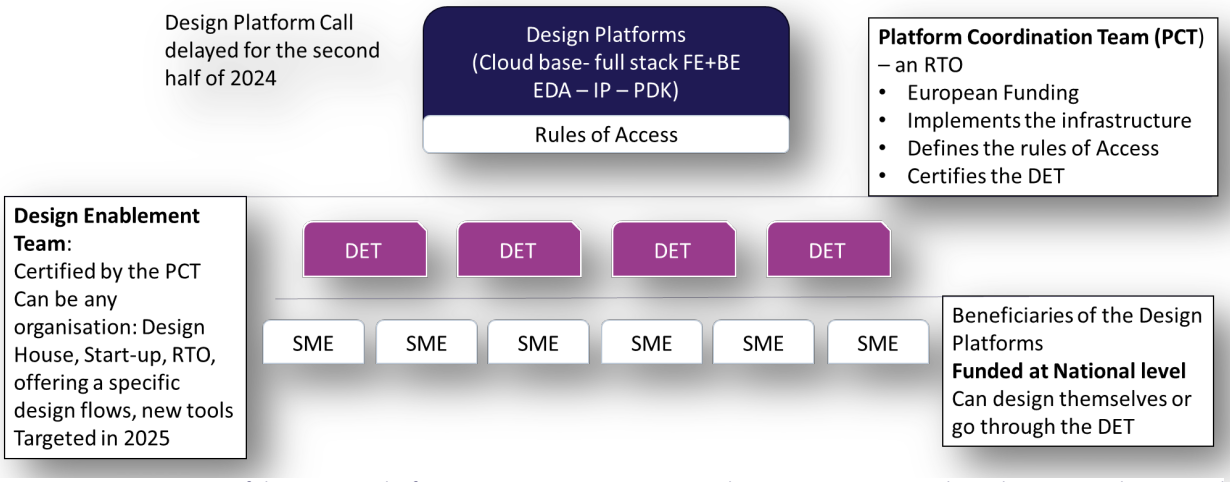

Figure 6: Organisation of the Design Platforms - Source itw CHIPS JU - this organisation may be subject to evolution until the publication of the call

Both the Advanced Packaging Pilot Lines and the Design Platform **will be pivotal tools** for the implementation of the Pack4EU strategy.

Strategic gaps

From the SWOT analysis we identified 9 strategic gaps to achieve our objectives.

- **Transfer path to the industry**

Europe is known for its high-quality research, it is also known for its difficulty to turn research into products and value. The investment in the CHIPS JU will create a strong Return on Investment if we pay a particular attention to this transition from the Research to the Industry.

- **Strategic Gap between Pillar 1 and Pillar 2 and 3 in the chips act**

This gap described in the Figure 5, also stresses the lack of connections between the research performed in the frame of the CHIPS JU and the future facilities which are not yet envisaged as collaboration partners.

- **Strategic Roadmap for advanced Packaging**

At the moment, there is no coordinated roadmap for the development of advanced packaging in Europe, Pack4EU initiate this effort both from the business traction and the technical aspects. A coordination with the industry (demand) and all the Pilot Lines is important to maintain. Synergies are possible with announced and future Pilot Lines (Photonics and Power Electronics Pilot Lines).

- **Design Ecosystem and Design rules in a Chiplet Architecture**

The Advanced packaging is currently mastered mainly by TSMC and INTEL and both organisations are vertically integrated. Designing a chiplet based system is currently only possible thanks to a coherent ecosystem of chiplets, which is only available from either INTEL or TSMC (exclusive or). To date it is not possible to design a chiplet concept from multiple vendor sources. Intel joined forces with Advanced Semiconductor Engineering Inc. (ASE), AMD, Arm, Google Cloud, Meta, Microsoft Corp., Qualcomm Inc., Samsung and Taiwan Semiconductor Manufacturing Co. to launch the Universal Chiplet Interconnect Express (UCIe) consortium. However, this effort will not be sufficient to serve the European Market with its specific needs. But the coherency across chiplets is missing, as well as design methodologies and flows, simulation, cybersecurity for chiplets...
And on the business side a real open marketplace is missing and the traceability of IP and business responsibility will need to be clarified. In order to implement advanced packaging for the European critical market, **it is crucial to break the vertical ecosystem barrier.**

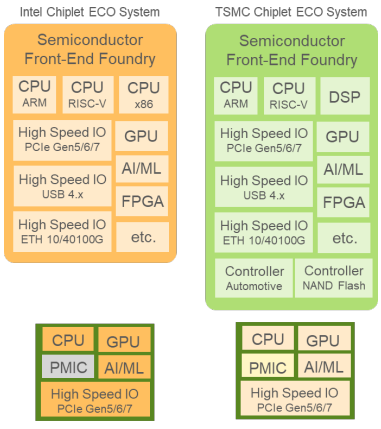

Figure 7: INTEL and TSMC closed ecosystem of Chiplets

- **Lack of industrial advanced packaging in Europe**

Advanced Packaging Technologies are strategic for the Artificial Intelligence market, and it is currently kept as an internal strategic resource by the IDMs (Figure 8). Only a limited spectrum of technology is currently mastered by the OSATs and it will be made available only for large volumes production. The Packaging facilities of INTEL announced in Europe, will serve only INTEL's need and Silicon Box is expected to serve only very large volume. Industrial source of Advanced Packaging technologies for European volumes/markets will not be available in the near future.

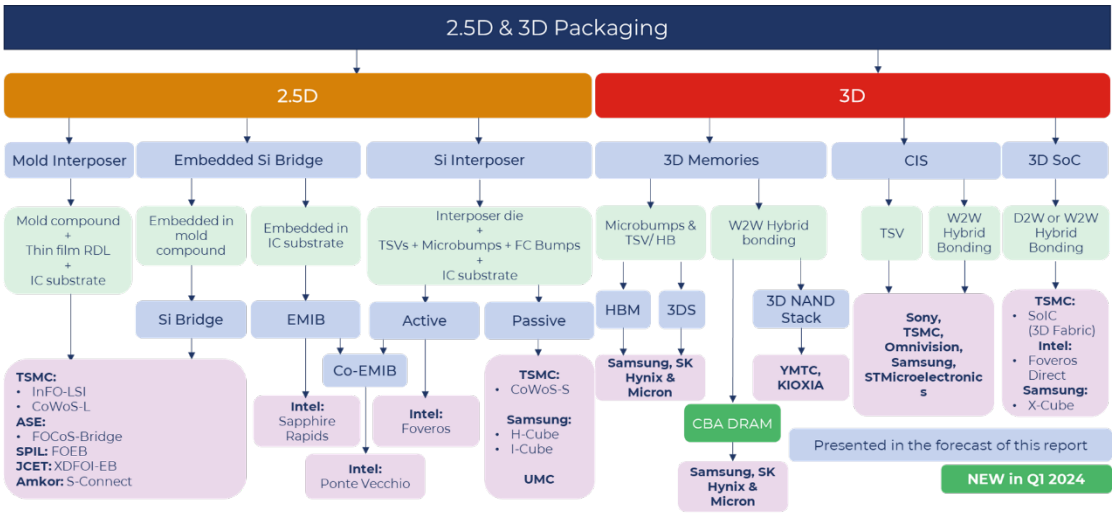

Figure 8: Advanced Packaging Technology owners

- **Fill the gap of the 100kUnits demand**

The current ecosystem of semiconductor packaging services in Europe can serve mostly small volumes from 1kpcs to 10kpcs per products which are typical volume for Defense or Medical applications. Large OSAT need to produce Millions of parts per product to make it economically viable. Lots of European Applications however will require intermediate volumes in the range of 100kpcs (e.g. radio base stations), these volumes are difficult to serve.

- **Support to SMEs**

The analysis of the funding breakdown in the former KDT JU projects has shown that the participation of SMEs could be improved (Figure 9). SMEs received less than 20% of the total funding when the number of participation of SMEs (125; 25%) is close to the number of participations for a large enterprise (165; 32%) . The participation of SMEs to the Chips JU is mainly driven by the large companies which lead the consortia. In addition, the level of technology mastered by European SMEs in packaging is far from the state of the art, yet perfectly adapted to the market demand. The incremental progress required doesn't perfectly match the topics supported in the Chips JU framework.

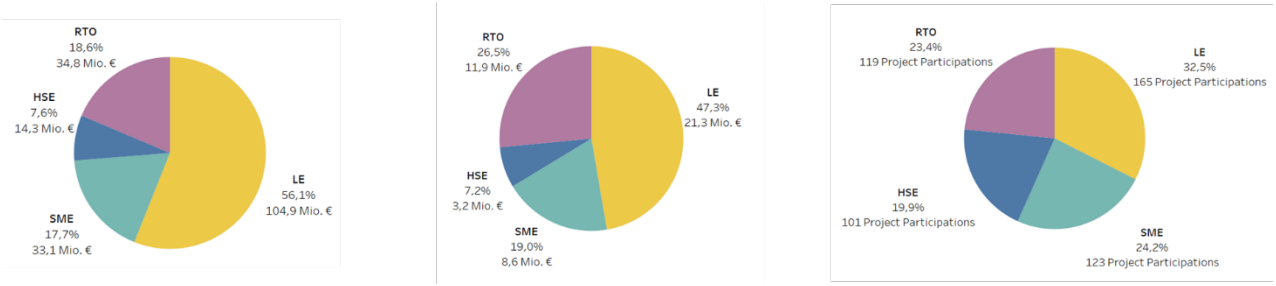

Figure 9: Total amount for KDT/ECSEL funded projects on packaging by actor and funding volume. (left) Total amount of EU contribution for KDT/ECSEL funded projects on packaging by actor and funding volume (Middle) Total project participations of EU contribution for KDT/ECSEL funded projects on packaging by actor (Right) HSE: Higher Secondary Education -RTO: Research and Technology Organisations – SME: Small and Medium Enterprises – LE: Large Enterprises

- **Skills and training**

The need for competencies in Packaging is a recuring request collected from the interviews performed both for the younger generation but also for the existing workforce to adapt to new technologies. From the survey performed by Pack4EU and the recent announcement in Poland (2000 jobs) and Italy (1600 jobs), we estimate that the need for new semiconductor packaging jobs is in the range of 6000 semiconductor packaging jobs in the near term.

- **Coordination**

Pack4EU started to federate the packaging community and the implementation of the advanced packaging strategic plan will require a strong federation of the European Packaging Community. A coordination of the efforts will also be required.

Technical roadmap

It has been established that the European market needs are extremely diverse. Each vertical business will require a specific set of technologies and we initiated a reflection on the needed technologies from the state of the art, mid-term and long-term. The needs in Power Electronics, Microwave, Photonics, Chiplet architectures, Quantum computing.

Power Electronics

One of the main driver for innovation in automotive is associated with the CO_2 Emissions and the needed transition to electrified powertrain and sharing schemes. The strongest driver for the EV/HEV market is the various governments' automotive CO2 emission reduction targets. Europe is the toughest market in which to sell polluting vehicles.

Consecutive to the automotive downturn initiated in 2023 followed by the Covid crisis in 2020 powertrain electrification has gained significant momentum in the rebound of 2021.
Plug-in Hybrid Electric Vehicle (PHEV) and Battery Electric Vehicle (BEV) combined:

- 13% market share has been reached in 2022
- 25% market share should be reached by 2025.
- 32% market share should be reached by 2028

This is driving the demand for innovation in Power electronics with other applications such as the high voltage power grid, high speed train and data centers.

The associated packaging challenges are about the management of :

- High voltage(>10 kV)
- High current (>1 kA)
- High temperature (>220°C)
- High thermal conductivity
- High insulation capacity

5G and Beyond

6G technology aims to significantly enhance the capabilities of 5G, increasing its efficiency by 10 to 100 times. This advancement will support extreme data rates, achieving up to 1000 Gbps, and provide ultra-low latency for instant communications, with latency as low as 0.1 milliseconds. Additionally, 6G will offer high-accuracy positioning within 1 cm. It will also integrate communications and sensing, enabling seamless communication from the network to sensors. Artificial Intelligence (AI) will be ubiquitous, operating at the edge and throughout the core network, benefiting from the development of fast and efficient quantum computing. Furthermore, 6G will ensure seamless communication between AIs, ranging from edge devices to high-performance computing systems.

The main capabilities expected from the 6G deployments are :

- Wireless Fronthaul/Backhaul: Point to point communication above 500Gbps at 100m or more
- Fixed Wireless Access: Point to multi-point links with fiber like speeds. Up to 20Gbps per users at 100m
- Short range D2D communications: Up to 50Gbps below 5m
- Mobile hotspot, Multi-user, Augmented and virtual reality: Point to mobile multi point communication 10 Gbps between 10 and 100m

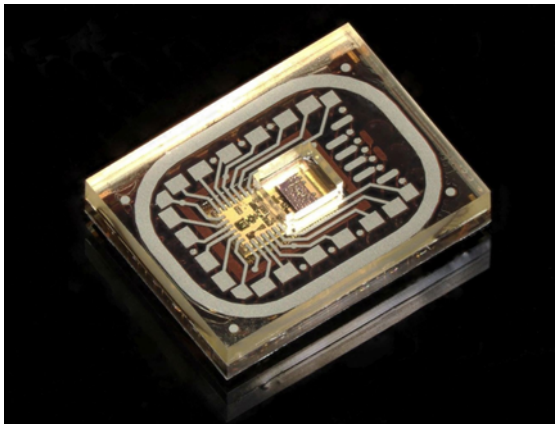

Figure 10: Radar sensors for industrial and process metrology (source Fraunhofer IZM)

Leading to the following packaging challenges for 5G and Beyond:

- High power efficiency/high-frequency bands/faster data transfer rates/low latency
- Extreme miniaturisation, high integration density, 3D integration
- Thermal management and reliability

Photonics

Photonics encompasses a broad range of applications, which can range from Imagers to Optical links. The latter can also be considered at the network level with broad range of fiber optics hierarchy from long haul to chip-to-chip optical interconnects. Silicon photonics is one of the major building blocks which is considered for the evolution of optical networks, but these technologies can also serve quantum computing and chiplet interconnects.

As we move towards co-packaged optics for optical communication, packaging is becoming more and more important for silicon photonics. Optical packaging mainly relates to the connection of optical fibers to the photonic integrated circuit. The two major challenges of optical packaging for PIC are: size adaptation (since the fiber diameter is 125 µm while the integrated waveguide diameter is a few µm) and modal adaptation. Electrical packaging relates to the electrical connection between chips and with the PCB. Two main approaches are now prevalent: 2.5D and 3D packaging.

The following packaging challenges are identified:

- On/off-chip optical coupling
- Packaging of laser sources
- Electronic-photonic-quantum co-packaging
- Thermal management
- Standardization & reliability

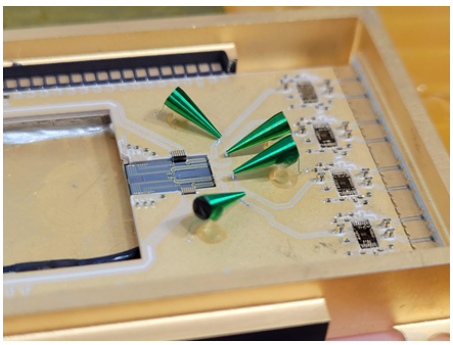

Figure 11: Photonics Integrated Circuit Packaging (Source: TYNDALL, PIXAPP)

Superconducting Quantum Computing

Quantum computing is an emerging market, and experts have differing opinions on how soon a quantum computer will be able to deliver useful results for practical applications. Various technical approaches are competing to produce qubits. Superconducting technology is the most mature and advanced, followed by cold ions or cold atoms, photonics, and silicon. While silicon offers scalability, it has only demonstrated very limited entanglement capabilities so far.

Roadmaps would be required for each and every technical option discussed above. In the present document we focus on the challenges associated with the Superconducting material requiring cooling[3].

The challenges for the superconducting quantum computing are the following:

- Gate fidelity, qubit lifetime, error correction
- Cryogenic interconnect, materials, 3D packaging
- Shielding and isolation (external noise & electromagnetic)
- Hybrid system integration of various qubits
- Quantum and electronic integration
- Standardization & reliability

2.5D – 3D for Chiplet architecture

The trend towards de-aggregation in silicon chips is driven by the increasing challenges associated with integrating multiple functions into a single chip. One major factor is the slowdown of Moore's Law, which traditionally predicted the doubling of transistors on a microchip every two years. Additionally, as silicon die sizes exceed the maximum reticle size, it becomes physically impossible to fabricate larger monolithic chips. Yield and cost limitations further complicate the production process, as larger dies typically have lower yields, making them more expensive to produce. Moreover, the skyrocketing cost of chip design is another critical factor, as the complexity and expense of designing highly integrated chips continue to rise. These challenges are pushing the industry towards de-aggregation, where functions are divided among multiple smaller chips or chiplets, which can be individually optimized and then integrated into a larger system.

Advanced packaging of Chiplets requires its own roadmap with short- and long-term goals associated with key milestones. There are numerous challenges behind the concept such as Signal integrity, Power integrity, cooling concept, Multi-die test concept, Organic interposers…and it can be implemented in a very broad range of concepts: Embedded Multi-die Interconnect Bridge (EMIB), Chip on Wafer on Substrate (CoWos), Integrated Fan Out (InFO).

Interconnects between chiplets is one of the major limitations and challenges in the concept. Parallel or Serial interface can be selected according to the targeted application (speed vs latency) but both

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3

A roadmap for quantum technologies in the UK (page 95,121, 157)
Strategic Research and Industry Agenda 2030, EU (page 130 - 135)
ASML's View of the Scaling Roadmap, Delft seminar HIR (page 18-19)
IBM roadmap, https://newsroom.ibm.com/2023-12-04-IBM-Debuts-Next-Generation-Quantum-Processor-IBM-Quantum-System-Two,-Extends-Roadmap-to-Advance-Era-of-Quantum-Utility

methods are operating at the physical limits. A transition to Optical interconnects is foreseen. It is studied at TSMC at a proof-of-concept level, and in Europe TYNDALL is working on similar objectives.

This Chiplet architecture is strategic for AI and Silicon innovation and is only mastered by a limited number of actors in the world. There is no open access to advanced packaging technologies in the world (Figure 8). In Europe, AT&S and Swissbit are targeting PCB as an advanced substrate for 2.5D integration (Figure 12)

The challenges for chiplet architecture packaging are:

- Architecture
- Interconnect bandwidth, interface, scalability
- KGD testing
- Thin wafers
- Signal & power integrity
- Integration passives
- Thermal management

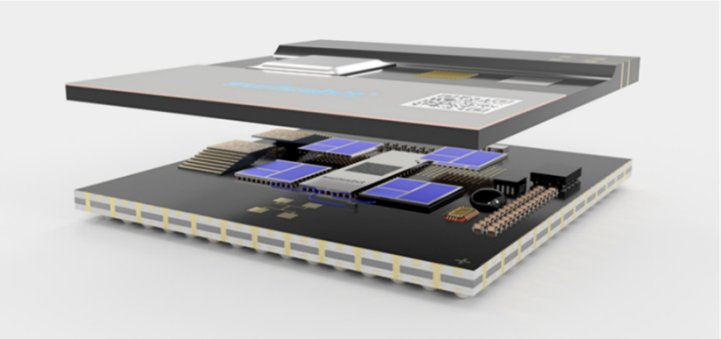

Figure 12: chiplet architecture without silicon interposer (source Swissbit)

European Packaging Roadmap

In this chapter we have covered some drafts of a number of strategic fields for Europe. This effort performed in Pack4EU is only a draft version of what is necessary for the exploitation of the Pilot Line in Advanced Packaging. A thorough effort is required combining the market demand and the translation of this needs in terms of technology building blocks to be developed in time.

Skills and Education

New investment in EU semiconductor back-end manufacturing facility will bring extra jobs. Intel announces investment in Italy to build a state-of-the-art back-end manufacturing facility. With a potential investment of up to 4.5 billion euros, this factory would create approximately 1,500 Intel jobs plus an additional 3,500 jobs across suppliers and partners, with operations to start between 2025 and 2027. Silicon Box will invest 3.2 billion euros in a new plant in northern Italy. At full capacity, the investment will be able to generate 1,600 new direct jobs. We believe that with the implementation of the EU Chips Act, there would be more new investment in the semiconductor industry and 10 times more additional jobs would be created.

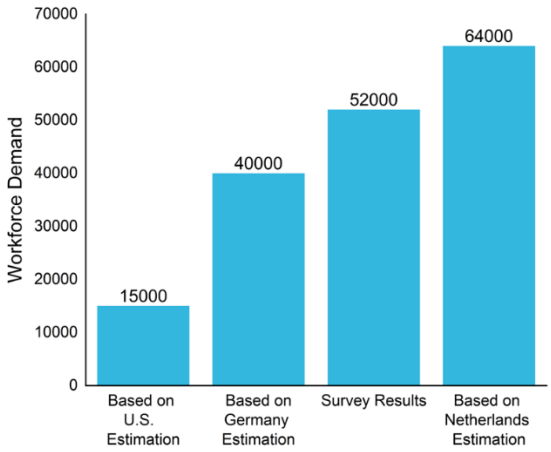

Figure 13: needs in packaging workforce depending on various means of estimation

Taking new investments into account, and depending on 4 different methods of estimation, between 15 000 to 64,000 workforces will be required for the EU packaging industry by 2030. This leads to an increase of training capacity in the range of + 500 engineers every year in the field of packaging compared to existing capacities.

Europe can not be compared to countries mentioned before with a central government funding centralised actions. Hence, coordinated strategies for education are difficult to arrive at as this is typical a national topic to shape education to the national needs.

Recommendations for skills and training:

1) Establish 8 specialized educational and training hubs for semiconductor packaging in Europe, located in Germany, France, the Netherlands, Italy, Spain, Poland, Eastern Europe, and Northern Europe.

2) Strengthen support for teaching staff development at national levels to enhance the recruitment and development of specialized teaching staff.

3) Establish a Unified European Roadmap and Educational System for Semiconductor Packaging Talent Development.

4) Open EU semiconductor pilot lines for packaging talent education and development, provide support for students' practical skills training.

5) Initiate some strategic partnerships with like minded countries for skills development and student exchange: US, Japan, Korea, Malaysia...

Design

Most of the packaging is considered as a commodity. But design is a good marker of Advanced Packaging. When co-design is needed between the chip and the package, this is where the packaging companies can deliver their added value. Design can draw the borderline between commodity and advanced solutions.

Chiplet Ecosystem

The design ecosystem is limited to closed ecosystems such as the INTEL or TSMC's. Some effort is in progress, led by INTEL to create a more open ecosystem. **T**he Universal Chiplet Interconnect Express (UCIe) is a key advancement for die-to-die interconnects, providing a standardized interface for efficient communication between chiplets. It ensures compatibility, high performance, and supports high-bandwidth, low-latency connections for computing applications. Another significant progress is the standardization of Electronic Design Automation (EDA) tools for high-speed digital link simulation, which are essential for designing and verifying interconnects between chiplets. They ensure signal integrity and performance, facilitating the development of reliable chiplet-based systems

Despite these advancements, several elements are missing. Maintaining coherency across chiplets is a challenge. Coherency ensures a consistent view of data across the system, which is crucial for performance and reliability. The lack of a standard approach can lead to inefficiencies. Additionally, standardized design methodologies and flows for chiplet integration, including comprehensive simulation tools, are lacking. These are needed to streamline the design process and ensure reliability. There is also no robust cybersecurity framework specifically for chiplets, including secure boot processes, encryption, and breach detection mechanisms. Developing this framework is crucial to protect chiplet-based systems.
Furthermore, standardized chiplet design templates and a generalized architecture framework would aid adoption. These would reduce complexity and ensure compatibility and interoperability, fostering a collaborative ecosystem.
On the business side, establishing a marketplace for chiplets would facilitate commercialization and adoption. It would enable designers to source and integrate chiplets from different vendors, fostering innovation and competition. Ensuring traceability of intellectual property (IP) and business responsibility is also critical. Maintaining detailed records of origin, ownership, and licensing enhances trust and accountability, ensuring compliance with regulations.

Ecodesign

As will be discussed in the next chapter, ecodesign is in its infancy and only basic design rules can be applied. It is necessary to integrate some true CO_2 footprint calculation that will include the suppliers' information such as the nature of the material and the level green energy consumption.

Standardization

For emerging markets such as Photonics and quantum, implementing standardization in the early stage of the design phase facilitates the deployment of the solutions. It has been implemented by PIXAPP where the Photonics Pilot Line included their design rules in existing EDA tools and it could be also implemented for future markets such as quantum computing.

Sustainability

Environmental concerns are largely driven by regulation. Companies either comply or use these regulations as marketing tools. Public-facing companies often emphasize sustainability, with leaders like Apple[4] influencing their supply chains. Smaller businesses typically follow regulations or customer expectations.

European regulations affect imported goods, specifying material nature but relying on local laws for manufacturing processes. Thus, customer commitment to the environment is crucial. European factories must comply with stringent local regulations, which can be advantageous for European customers but challenging for others.

Sustainability is a high-end concern driven by regulations and customer pressure, with customer demands affecting the entire value chain.

The automotive industry in Europe has begun including CO_2 footprints in Requests for Quotation, leading to cascading supplier demands. GHG protocols are used, with Scope 3 being the most challenging, often estimated through public databases. Tools like GaBi from Sphera Solutions are widely used, though different databases can yield varying results. Ultimately, supplier differentiation relies on platforms like CDP.net, where companies disclose their carbon footprints. However, current methodologies lack product-level assessments, relying instead on approximations based on company revenue and component prices[5] . In addition, material CO_2 footprint management is complex due to varying finishing processes impacting CO_2 footprints.

Key takeaways:
- Scope 3 is calculated, with no bottom-up methodology.
- Suppliers are differentiated at a corporate level, not product-specific.
- Eco-design is nascent.
- Sustainability is driven by European OEMs but doesn't necessarily lead to European factory relocations, including Packaging factories.

Advanced packaging is emerging as a solution to the limitations of Moore's Law, with hybrid integration improving yield and reducing costs. Fraunhofer studies show CO_2 footprints are more concentrated in the front end due to more steps and infrastructure. That’s why Yield and Reliability are key elements to study in Packaging to secure the large CO_2 footprint created in front end.
Future efforts should focus on sustainable materials, traceability, and eco-design. Knowing the strong dependence of Europe with regard to electronics materials, International collaborations are necessary to transform the industry.

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[4] Silicon greatly impacts a company's carbon footprint. For Apple, one-third of emissions are in integrated circuits.
[5] The ratio between revenue and Product price is applied to the full Carbon footprint of the company to deduce the Carbon footprint of the product.

International Collaboration

The question of international collaboration in research is managed at many different levels. During the Pack4EU project, we were invited to contribute to the analysis conducted by DG Research & Innovation and we also had multiple interactions with the ICOS project.

From the work performed by DG Research & Innovation to ICOS and our contribution, the focus becomes progressively narrower, but semiconductor packaging remains a recurrent topic in many discussions, indicating its importance.

The list of countries considered is the following:

- USA
- Japan
- South Korea
- Taiwan
- China
- Malaysia

Some initiatives are in progress (Korea) or will be in the short term (Japan) in the frame of the CHIPS JU and Heterogeneous Integration and sustainable material should be considered as a priority topic.

Mid-term opportunities are possible with USA and a strong interest was expressed from our counterparts in the country. Pack4EU created the connection with the ICOS project for the follow-up of the initiated relationship with the University of Arizona in Phoenix.

Even though some important progress were made in the relationship with China, it is difficult to envision a short-term implication of Chinese research organization in European Projects. The situation with China is conditioning the collaboration with Taiwanese organizations as well. These partnerships will be only long term.

In South East Asia, the priority of the ICOS project is on Singapore, however for Advanced Packaging, we recommend to **consider Malaysia as well due to their competencies in Packaging and their willingness to progress in design**. It also appears possible to build a win-win relationship with this country considered as a “safe harbor” by numerous European and US companies.

Multiple technical topics can be considered for international relationship **but skills and training** should also be considered to stimulate the attractivity of the Semiconductor business. In addition, the excellence of the European research can also be considered as a trading option for the security of supply.

Strategic plan and recommendations

In the following section we will describe a series of recommendations which are organized in 3 sections:

- Infrastructure
- Funding instruments
- Governance

The picture below is a representation on how these organisms and Instruments are connected and work together.

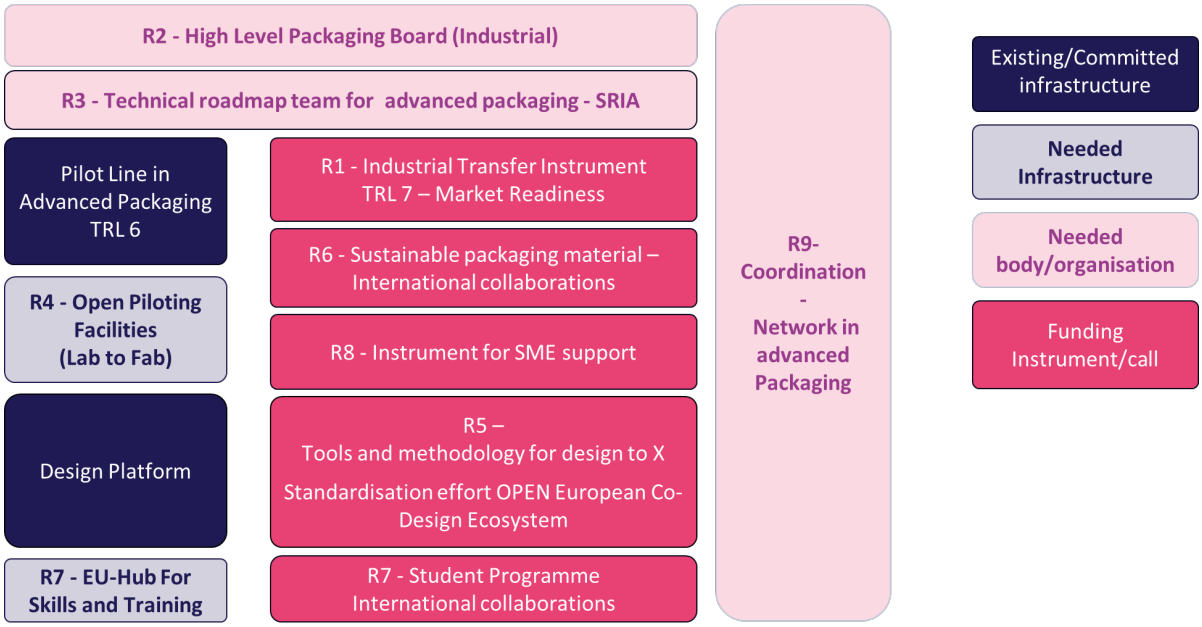

Figure 14: European Strategy for Advanced Packaging: Mapping of recommendations

Recommendation 1: Implementation of an Industrial Transfer Instrument for semiconductor packaging bridging the gap between prototyping and production.

The transition of the Pilot Line to the Industry requires a particular attention and should be taken into account in the CHIPS JU project to make sure the initial investment is properly exploited (cf. The CHIPS JU tools). The research organisations have cumulated a broad range of know-how and IP from former KDT projects, it is then possible to initiate this effort ahead of the full deployment of the Pilot Line which may require 3 years before it can be fully operational.

We estimate that projects consortia with a budget ranging from 30 to 50M€ per project with a total of 100M€ split between 2025 and 2027, would permit to generate the necessary return on investment on the "backlog IP". These projects would aim at a direct transfer to the industry.

Recommendation 2: Establish a High-Level Packaging Board composed of industry leaders to guide strategic directions driven by market needs, ensuring innovation in packaging standards and practices

As discussed in the chapter dedicated to The CHIPS JU tools there is a structural gap between the Pillar 1 and Pillars 2-3. To avoid the isolation of research from the market demand, we recommend the creation of a High-Level Packaging Board composed of Industry leaders. The board would be established from Industry Experts whose role will be to guide strategic directions driven by market needs, ensuring innovation in packaging standards and practices.

Recommendation 3: Implementation of a technical expert group for developing and updating a Roadmap for Advanced Packaging in Europe.

The technical expert group is an open group of packaging experts from RTOs and universities (pilot line owners, partners and others) and experts from industry (LEs, SMEs, start-ups) across Europe.

The objectives of the working group are:

- Development of a European Packaging Roadmaps
- Action plan(s): how to make best use of the pilot line on heterogeneous integration
- Accelerate the Lab to Fab transfer
- Monitoring of the project results and RoI
- Assessment and revision of the roadmap creating a feedback loop for the Pilot Line

In a first step, we will ask associated partners of the Pack4EU, the EPoSS Task Force on Advanced packaging members and representatives of the pilot line on heterogeneous integration to join the Expert Group.

EPoSS office will manage the process (set up regular meetings and draft the program and report to the ECS SRIA team regularly). In a first workshop on June 26, Fraunhofer introduced the capabilities of the PL to the experts.

The idea is to start with the “Chiplet integration technologies” roadmap and action plan as the hottest topic for Europe and to develop a work program towards a European Chiplet integration platform using the existing capabilities and later the future capabilities of the pilot line and the design platform.

Next steps will be other packaging topics where Europe should commonly be faster and set new standards (e.g. power packaging, photonics, RF/mmWave….).

Recommendation 4: Creation of Open Piloting Facilities for small and medium volume production as a seed for growing European Advanced Packaging capabilities.

Motivation

From interviews performed with the candidates for the Pilot Line call6, it was stressed that the research organisation could not perform activities beyond TRL5. Given the structure of the Research Organisation, studies on yield or reliability could not be performed and are considered beyond the mission of an RTO.

Open Piloting Facilities

Consequently, to fully comply with the objectives of the CHIPS JU and manage the delivery of small series of products, but also to create a smooth transition from the lab to the fab we recommend the creation of Open Piloting Facilities which would supplement and continue the effort of Pilot Lines. Building blocks reaching a TRL5 could be transferred to facilities to be implemented for productisation.

These Facilities would host a Production line that will be used in a Pilot mode. It will be open to Industry for projects and small series production, it can also serve as an OSAT for SMEs. The essential element of the infrastructure will be its openness to the European Ecosystem. Multiple models can be considered:

- **Access to machines**: workers from a company will have access to the equipment for training or to conduct their own development or small production.
- **Access to machines and competencies**: in this model, the Piloting facility will provide the required competencies for similar missions.
- **Subcontracting in technology maturation**: in a model similar to the RTO, the Piloting facility could conduct maturation studies to test equipment, processes or materials in a larger scale.
- **Small series production and test**: the facility would act as an OSAT for small series production.

In the long term, in a 10 years (or less) timeframe the Piloting facility could become a European OSAT securing the critical needs in advanced packaging for Europe. The business model could be modulated according to the customer's willingness to share data with the community.

Such a Piloting Facility would work according to industrial standards and each project started on the line is potentially a product that will enter into production in a short timeframe. This means that progressively, the line will operate with a mixed model of Production and Pilot.

Missing capabilities

A number of supply chains are already in place and we do not expect any specific needs in packaging for small businesses. The power electronics supply chain for example is managed by IDMs (Integrated Device Manufacturers) to maximize value. For sensors, there are established OSAT (Outsourced Semiconductor Assembly and Test) facilities in Europe and globally to ensure broad coverage and

[6] Interview M. Patrick Bressler for his participation to the January 2024 Associated Partner Meeting

reliability. Additionally, we have a robust supply chain in place for RF (radio frequency) components, supporting a comprehensive European needs.

The markets in photonics and quantum computing can be considered as more distant needs.

There are however clear missing capabilities for the chiplet ecosystem. Some Advanced Packaging technologies are available from OSATs for large volume, and we might expect some capacities from the future factory of Silicon Box in Italy. However, **there are no Open Facilities for the European needs capable to deliver small and medium volumes.**

A progressive implementation from Proof of Concept to Full Pilot

We estimate that the total investment for a Chiplet packaging facility is in the range of 150-200M€. Investments could be initiated with a first instalment of 15 M€ and following milestones achievement and concepts demonstrations could be further supported in multiple instalments. These figures have been collected through interviews of similar initiatives in the US and a German cluster of industrial companies ready to contribute to the initiative.

A Public Private Partnership to secure the European Market

The initiative must be implemented in the frame of Public Private Partnership with a number of Founding companies who would commit to invest in such Piloting Facility. To date a first industrial consortium composed of Swissbit and AEMTEC is ready to support and invest, others are in discussion and might follow.

With the proper organisation, one of the missions of this facility would be to fill the gap for 100kUnits.

This concept would enable the secure production in Europe of critical components for the European industry. As described above, this facility could be developed with its own business model with a gradual transition towards a production facility within 10 years.

A role model in Digital and Sustainability

The facility will be state of the art both in terms of Digital capabilities with locally connected machines, data storage, Edge Computing capability and Digital Twin implementation. The Pilot Line in Fraunhofer will be capable of a proof of concept for the digital technologies to be implemented. The digitalisation of the 11 facilities through the FMD is a solid base in this direction. The monitoring of the facility will enable the implementation of an Ideal Fab targeting a state-of-the-art facility. The real time collection of the data **will support the construction of a bottom-up model for traceability of semiconductor products with a European Product Passport implementation.**

This action will be supported by the existing research effort and through the Acceleration/Transfer projects.

A Sandbox for Equipment Start-ups

The European ecosystem of start-ups in packaging are positioned quite well with equipment companies such as Lidratec or 3Dis and others. The first customers are difficult to find due to the difficulty to guarantee the high throughput expected in a production environment. The Pilot Line and

Piloting Facilities are two ideal opportunities for European start-ups to showcase their equipment and demonstrate the capabilities in real settings and to improve their equipment.

No specific budget estimate is given here, but we consider that the budget allocated to the existing and to be stablished infrastructures should open the door to future European champions.

Recommendation 5: Development of tools and methodologies for a Design-to-X approach & Standardisation for an OPEN European Co-Design Ecosystem.

Stategy for Design Platforms in Advanced Packaging

A design to X approach

Since the Pilot Line will most likely be limited to activities below TRL6, topics like yield and reliability are not addressed in this context. Those aspects are however key for a successful industrialisation, the huge success of the Asian suppliers rely mostly on their capability to achieve high yield. In addition, yield is essential for the carbon footprint of the final product. The whole front-end process could be considered as a huge CO2 investment, which could be lost if yield is low in the back-end steps.

This is the reason why, as an overarching principle to the Design Platform, we believe it is important to initiate design through a Design to X principle, where X could stand for Yield, Reliability, Manufacturability, Sustainability. There are many trade-offs to be considered and cycle time to market could be shorten with the appropriate anticipation at the design level.

European OSATs referenced Design Kits

To give a higher visibility to the European packaging industry, it is advised that each organisation willing to benefit from more visibility, shares a set of design rules and capabilities which could direct the designers towards a particular supplier. This action can be managed by the competence centres in coordination with the Platform Coordination Team.

This standardisation effort can beneficial also for the Emerging markets such as Photonics and Quantum in order to facilitate the future implementations.

A European Open Ecosystem for Advanced Packaging co-design

In order to break the Vertical Integration Ecosystem, it is of utmost importance to create an Open European ecosystem in design. Like the RISC-V Open-Source ecosystem is becoming a relevant alternative to the monopoly of ARM, Europe needs to build the open-source design libraries that will enable the creation of a coherent ecosystem of chiplets to be integrated as System on Chips through advanced packaging. What is missing in vertical integration will be balanced with a more fragmented Start-up/SME ecosystem of design houses and product designers.

Recommendation 6: Consolidate international relationships through open calls on Sustainable Packaging Materials and Substrates.

Europe is facing a strong dependency on Material since it is a highly concentrated market with 77% of the material and substrates originated from Japan, cumulating to 84% with the additional market share of South Korea (Figure 1: Breakdown of the Semiconductor market per geographical area - Source Yole développement. OSAT are concentrated in TW and CN, Material are concentrated in JP and SK. Material and Substrates are key for the implementation of an advanced packaging. It is then necessary to take some mitigating measures with dedicated programs focussing on these topics.

An opportunity for International Collaboration

As previously said, Japan is the partner which should be targeted material related topics. From interactions with the I-COS CSA it appears that heterogeneous integration is one of the topics often identified among the potential subject of interest both with South Korea and Japan. A first call is in progress with South Korea where heterogenous integration is explicitly mentioned. The next targeted collaboration being with Japan, the topics of Sustainable Manufacturing as well as Heterogeneous Integration should open a potential for a more secure sourcing of Sustainable Material.

An interview has been conducted Abe-san, CTO of the leading material supplier RESONAC from Japan. The company as developed a collaboration with the US would be open to discuss options in Europe. A win-win collaboration could take place on materials for automotive power packaging.

Recommendation 7: Bridging research and education and facilitating international exchange on training through an EU Education Hub :

Building a framework for access to EU-funded research pilot lines for students

Develop International collaboration for training and skills in advanced packaging

Recent announcements of INTEL for POLAND projects the creation of 2000 semiconductor jobs in advanced packaging. The creation of a Silicon Box Factory in the North of Italy will create 1600 additional jobs. In addition, from the survey conducted by Pack4EU we estimate a total short-term need of 6000 semiconductor packaging jobs. The needs are evenly distributed between engineers, researchers and technicians. It could be considered that 1000 students should be trained every year to the specific needs of packaging. The effort in education is a National Policy question, however, the upcoming INTEL facility is not necessarily positioned in a hot spot for Packaging and Europe can help with Cross border Initiatives.

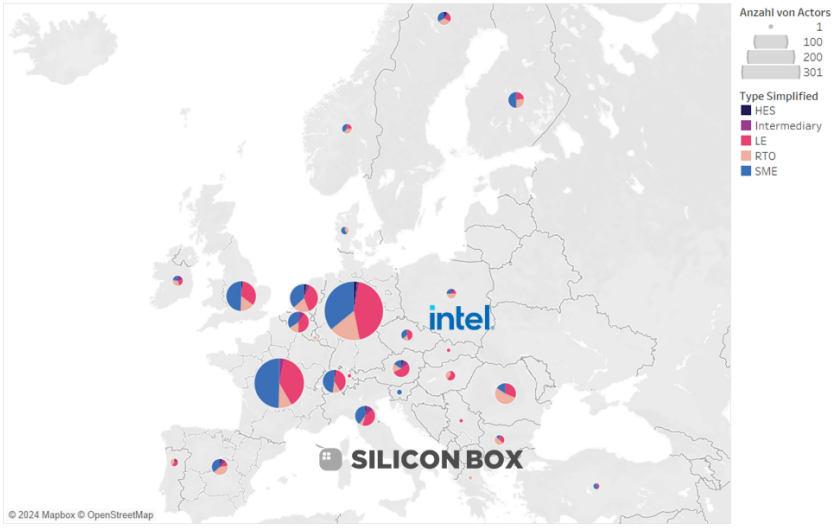

Figure 15: Mapping of the European Competencies in Packaging. Recent addition of INTEL and SILICON BOX projects

A program for the mobility of students in Europe to have access to the right expertise and facilities would permit the training of engineers through short research projects. This would create a bridge between University and Research. The access of students to the Pilot Line or Piloting Facility is a way to train future workers needed in the industry. The number of trainings is however important and could be beyond the capacity of the facilities themselves. A research university like the Tohoku University in Japan trains 100 students per year. The numbers are collected by the Japanese Ministry of Education and consolidated to monitor the progresses.

From these numbers, it is necessary to identify in the range of 10 training spots throughout Europe and supplement the existing recruitment of local students with mobility scholarship. A monitoring of the number of students trained should be collected through the network of Competence Centres and reported to the CHIPS JU.

Given the expected numbers, this measure might remain insufficient, and it there is then a need to identify the Competent Universities who do have the Fundamental knowledge, but lack of the specific expertise for packaging and offer specific programs for Packaging specialisation.

Countries like Malaysia train about 40 000 semiconductor professionals every year. An international exchange programme could enable the creation of long-term bridges between Europe and Malaysia which is considered as a “safe harbour” by the industry. Our discussions with the University of Arizona has shown also the same openness to create synergies in training or student exchanges.

We estimate that a budget **of 6M€/year over 3 years**, a total of 600 students would benefit from a high-end training in addition to the existing capacities. This budget would include the living expenses and would not cover the Project research.

In addition to the training of a new generation of young engineers, we also collected concerns and interest from the industry for a continuous training of professionals for new methods and technologies for the upgrade of the current workforce. This aspect will be further debated in the consortium. While

the channels for training might be the same (universities and RTOs), the financing of continuous training varies from one country to another depending on legal obligations applicable to the employers.

Recommendation 8: A Support for Small and Medium Enterprises through dedicated open calls applying cascade funding schemes.

As mentioned higher in the document, SMEs participation to the CHIPS JU could be improved. The participation of SMEs in the CHIPS JU are mainly driven by the large corporates. The support of the remaining European Ecosystem in packaging could benefit from a specific instrument for SMEs to support them in their technology roadmap.

Our analysis of the past budget of SMEs in Packaging in the KDT JU shows a budget of 33.1M€ (source KDT). We consider that such an instrument could support the industry with a budget of 60M€ split in 2 calls, for SMEs with a low participation rate in the previous projects. The Cascade Funding Scheme applied in Horizon Europe has proven to be very successful to tackle very specific problems. An adaptation of such a framework for the CHIPS JU could be a solution to attract newcomers in the European Collaborative Research ecosystem.

Recommendation 9: Creation of a Pan-European Network for Advanced Packaging to federate and strengthen the European ecosystem

For the proper implementation of the strategy, an effort of federation and coordination is necessary. The creation of the Pan-European network is an objective of Pack4EU and will be launched at the final event.

The mission of the Pan-European Network will be to federate the industry on a common roadmap which will be established through the Expert Group. It will consolidate the vision of the existing organisations and also maintain a survey on the European forces in play in the field. A CSA will be needed to support this network. A four-year project that will follow the progress until the implementation of the Pilot Line and Piloting Facility.

Conclusion

The European semiconductor ecosystem must prioritize strategic investments in Packaging R&D and an open production facility to address the diverse and fragmented needs of the European market. With varying requirements across sectors such as automotive, telecom, industry, sovereign markets, and medical, tailored approaches to innovation are essential.

The semiconductor innovation is shifting towards back-end processing, with advanced packaging emerging as the next significant milestone. This shift addresses the growing complexity and performance demands of modern electronic devices, driven by the need for higher integration, improved performance, and greater efficiency.

Technologies such as 2.5D and 3D integration, chiplet architectures, and photonics integration are crucial for ADAS application, RF or telecommunications. These technologies enable the creation of highly integrated systems that deliver superior performance, reduced power consumption, and enhanced functionality. A preliminary roadmap has been drafted during the Pack4EU duration. It is now necessary to engage the industry and research community in the consolidation of roadmaps driven by market demand.

A significant challenge relies in the technology transfer from Research organizations towards the European semiconductor industry, but also the absence of open facilities capable of delivering advanced packaging technologies within the next 3 to 10 years. These gaps threaten Europe's ability to develop and commercialize innovative solutions. Europe must invest in technology transfer and in establishing open facilities with the necessary infrastructure, resources, and collaborative environment to support the development and scaling of advanced packaging-based products.

To achieve this, it is equally important to federate the European Union's capacity in training to supply the necessary workforce. This involves enhancing educational programs, creating specialized training hubs, and develop international collaborations.

Digitalisation and sustainability remain important challenges for Europe, it is also an opportunity to initiate collaboration with like-minded countries to secure the sourcing and development of sustainable materials.

SMEs are supplying strategic and sovereign businesses and are not sufficiently present in CHIPS JU projects. Dedicated funding instruments are necessary to support this ecosystem with their technical roadmap.

One of the great achievements of the Pack4EU initiative has been to federate the Packaging community and this will be continued through the coordination of the Pack4EU network.